PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/626,507
Filing Date:	07/24/2003
Applicant:	Son Ho et al.
Group Art Unit:	2188
Examiner:	Kaushikkumar Patel
Title:	LINE CACHE CONTROLLER
Attorney Docket:	MP0390

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PRE-APPEAL BRIEF REQUEST FOR REVIEW AND PETITION FOR EXTENSION OF TIME

Applicants request a Pre-Appeal Brief Conference and contend that the combination of Zaidi (U.S. Patent No. 6,601,126) with any other reference of record fails to teach or suggest the elements of the presently pending claims. Further, Applicants contend that the elements are not inherent in the cited references.

Applicants hereby petition under the provisions of 37 C.F.R. § 1.136(a) for an extension of time in which to respond to the outstanding Office Action and includes a fee as set forth in 37 C.F.R. § 1.17(a) with this response for such extension of time.

STATUS OF CLAIMS

Claims 1-5, 11, 13-15, 20, 44-48, 50, 52-54, 79-83, 89, 91-92 and 97 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1) and Jim Handy (The Cache Memory Book, second edition, published 1998) and Taylor et al. (U.S. Pat. No. 5,699,551). Claims 16-18, 32-38, 55-57, 67-73, 93-95 and 109-115 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998) and Taylor et al. (U.S. Pat. No. 5,699,551) in further view of Bryant et al. (U.S. Pat. No. 4,008,460). Claims 19, 58 and 96 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998),Taylor et al. (U.S. Pat. No. 5,699,551) and Barroso et al. (U.S. Pat. No. 6,725,334 B2) in further view of Veidenbaum et al. (Adapting Cache Line Size to Application Behavior, pub. 1999). Claims 12, 29, 39, 51, 64, 74, 90, 106 and 116 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaidi et al. (U.S. Pat. No. 6,601,126 B1), Jim Handy (The Cache Memory Book, second edition, published 1998),Taylor et al. (U.S. Pat. No. 5,699,551) and Barroso et al. (U.S. Pat. No. 6,725,334 B2) in further view of Ebner et al. (U.S. Pat. No. 6,928,525).

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a line cache control system. The line cache control system includes a line cache and a switch that selectively connects the line cache to one of first and second memory interfaces based on a memory select portion of an address. The switch includes **a plurality of selectors that each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address**. The remaining independent claims recite similar subject matter.

ARGUMENT

Applicants submit that Zaidi, either singly or in combination with any of the other cited prior art references, fails to at least show, teach, or suggest that said switch includes a plurality of selectors that each receive the second address and each select between first and second sets of signals relating to the first and second memory devices, respectively, based on the second address, and further submit that this structure is not inherent in the other cited prior art references.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, the alleged combination fails to disclose the limitation that the switch includes a plurality of selectors that each select between first and second sets of signals relating to the first and second memory devices based on the second address.

As shown in exemplary embodiments in FIGS. 6 and 7 of the present application, a switch 268 includes a first multiplexer/selector 244 that receives a memory select signal lc_addr[24] and selects between a buffer clock signal bf_clk and a flash clock signal f_clk accordingly. A second multiplexer/selector 246 receives the memory select signal lc_addr[24] and selectively outputs a signal to a buffer interface or a flash interface. A third multiplexer/selector 248 receives the memory select signal lc_addr[24] and selects between buffer and flash acknowledgment signals. In other words, the switch includes a plurality of selectors that each select between first and second sets of signals relating to the first and second memory devices based on the memory select signal (e.g. based on the second address). As best understood by Applicants, Zaidi fails to disclose this limitation. (See Pages 36-37 of Applicants' response filed March 5, 2007).

The Examiner **acknowledges that neither Zaidi nor any other cited reference explicitly discloses this limitation, and instead alleges that this**

structure is inherent. Applicants respectfully submit that the Examiner has failed to support a prima facie case for inherency.

The Examiner admits that the Zaidi, Jim Handy, and Taylor references are silent as to a plurality of selectors that each select between the recited first and second sets of signals. Instead, the Examiner notes that Zaidi teaches CPUs connected to either SRAM or flash memory through a switched channel memory controller, and the selection of respective signals is inherent. (See Page 5, Line 18 through Page 6, Line 5 of the Office Action mailed May 2, 2007). Applicants respectfully note that the Examiner relies on a MAC 140 to disclose the claimed switch and the plurality of selectors. Applicants submit that a MAC does not necessarily include a plurality of selectors as Applicants' claims recite.

Applicants note that the fact that a certain characteristic **may occur or be present** in the prior art reference is not sufficient to establish inherency of that characteristic. ***In re Rijckaert***, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (emphasis added). The Federal Circuit has clearly stated that:

> To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is **necessarily** present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities.'

In re Robertson, 49 USPPQ2d 1949, 1950-1951 (Fed. Cir. 1999) (emphasis added).

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic **necessarily** flows from the teachings of the applied prior art." ***Ex Parte Levy***, 17 USPQ2d 1461 (Bd. Pat. App. & Inter. 1990) (emphasis original). Therefore, in order to maintain a valid inherency argument it must be shown that the MAC 140 including the plurality of selectors must **necessarily** flow from the teachings of the Zaidi reference. Applicants respectfully assert that this is not the case here. In particular, Applicants note that a MAC does not necessarily include a plurality of selectors arranged as

recited in the claims, and the Examiner fails to provide any reference to support this allegation.

The Examiner further notes that Jeddeloh discloses that a switch 160 "can be a set of multiplexers." (Page 6, Lines 5-10 of the Office Action). Applicants respectfully note that the claims recite that the plurality of selectors **each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address**, and a mere reference to a set of multiplexers fails to disclose the specific structure of this limitation.

Therefore, Applicants respectfully assert that the Examiner has failed to properly support his rejection under either 35 U.S.C. §103 and/or 35 U.S.C. §103 with an inherency argument. Applicants respectfully submit that Zaidi, either singly or in combination with Jeddeloh or any other cited reference, discloses a plurality of selectors that each receive the address and select between first and second sets of signals relating to first and second memory devices based on the address. Applicants further submit that Examiner has failed to support his allegation that this structure is inherent in either Zaidi or Jeddeloh. Accordingly, Applicants respectfully submit that the presently pending claims are in condition for allowance.

Respectfully submitted,

Dated: August 23, 2007

By: _____

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